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IN THE CLAIMS:

The following listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently Amended) A ferroelectric memory device comprising:

a memory cell array, in which memory cells are arranged in a matrix, including first signal electrodes, second signal electrodes arranged in a direction intersecting the first signal electrodes, and a ferroelectric layer disposed at least in intersection regions between the first signal electrodes and the second signal electrodes; and

a peripheral circuit section for selectively performing information write or information read with respect to the memory cells,

wherein the memory cell array and the peripheral circuit section are disposed in different layers, and

wherein a portion of the memory cell array vertically overlaps the peripheral circuit section.

2. (Original) The ferroelectric memory device according to claim 1,

wherein the memory cell array and the peripheral circuit section are layered on a single semiconductor substrate in order from the peripheral circuit section to the memory cell array.

3-5. (Cancelled)

6. (Original) The ferroelectric memory device according to claim 1,

wherein the memory cell array comprises an underlying layer formed of a ferroelectric material or a material having a crystal structure similar to a structure of a ferroelectric, the first signal electrodes, the ferroelectric layer, and the second signal electrodes which are layered on a substrate.

7. (Previously Presented) The ferroelectric memory device according to claim 1,

wherein the memory cell array comprises an insulating substrate, the first signal electrodes provided in grooves formed in the insulating substrate, the ferroelectric layer and the second signal electrodes are layered on the insulating substrate on which the first signal electrodes are formed.

8. (Original) The ferroelectric memory device according to claim 1,

wherein the memory cell array comprises an insulating substrate on which is formed depressed portions and projected portions in a given pattern, the first signal electrodes are formed at a bottom of the depressed portions and an upper side of the projected portions, and the ferroelectric layer and the second signal electrodes are layered on the insulating substrate on which the first signal electrodes are formed.

9. (Previously Presented) The ferroelectric memory device according to claim 1,

wherein the memory cell array comprises an insulating substrate on which is formed the first signal electrodes, the ferroelectric layers, and the second signal electrodes, the ferroelectric layer is formed in a divided manner and disposed in the intersection regions between the first signal electrodes and the second signal electrodes, and dielectric layers differing from the ferroelectric layers are formed between the adjacent divided ferroelectric layers.

10. (Currently Amended) The ferroelectric memory device according to claim ~~9~~ 6,

wherein the dielectric layers are formed of a material with a dielectric constant smaller than a dielectric constant of the ferroelectric layer.

11. (Previously Presented) A ferroelectric memory device comprising a plurality of unit blocks of ferroelectric memory devices according to claim 1 arranged in a given pattern.

12-13. (Cancelled)

14. (Currently Amended) A ferroelectric memory device comprising a plurality of sets of ~~a~~ ferroelectric memory ~~cell array and a peripheral circuit section~~ devices according to claim 1 layered on an insulating substrate.

15-19. (Cancelled)

20. (New) A ferroelectric memory device comprising a plurality of unit blocks of ferroelectric memory devices according to claim 2 arranged in a given pattern.

21. (New) A ferroelectric memory device comprising a plurality of unit blocks of ferroelectric memory devices according to claim 6 arranged in a given pattern.

22. (New) A ferroelectric memory device comprising a plurality of unit blocks of ferroelectric memory devices according to claim 7 arranged in a given pattern.

23. (New) A ferroelectric memory device comprising a plurality of sets of ferroelectric memory devices according to claim 2 layered on an insulating substrate.

24. (New) A ferroelectric memory device comprising a plurality of sets of ferroelectric memory devices according to claim 6 layered on an insulating substrate.

25. (New) A ferroelectric memory device comprising a plurality of sets of ferroelectric memory devices according to claim 7 layered on an insulating substrate.